2 T881 Circuit Operation

This section provides a basic description of the circuit operation of the T881 transmitter.

Note: Unless otherwise specified, the term "PGM800Win" used in this and following sections refers to version 3.00 and later of the software.

Refer to Section 6 where the parts lists, grid reference index and diagrams will provide detailed information on identifying and locating components and test points on the main PCB.

The following topics are covered in this section.

2.1   Introduction

The individual circuit blocks which make up the T881 are:

- synthesiser

- VCO

- audio processor

- power amplifier (RF power module)

- voltage regulators.

Each of these circuit blocks is set in its own shielded compartment, formed as an integral part of the main chassis.

The configuration of the circuit blocks may be seen on a functional level in Figure 2.1. Refer to the circuit diagrams in Section 6.2 for more detail.
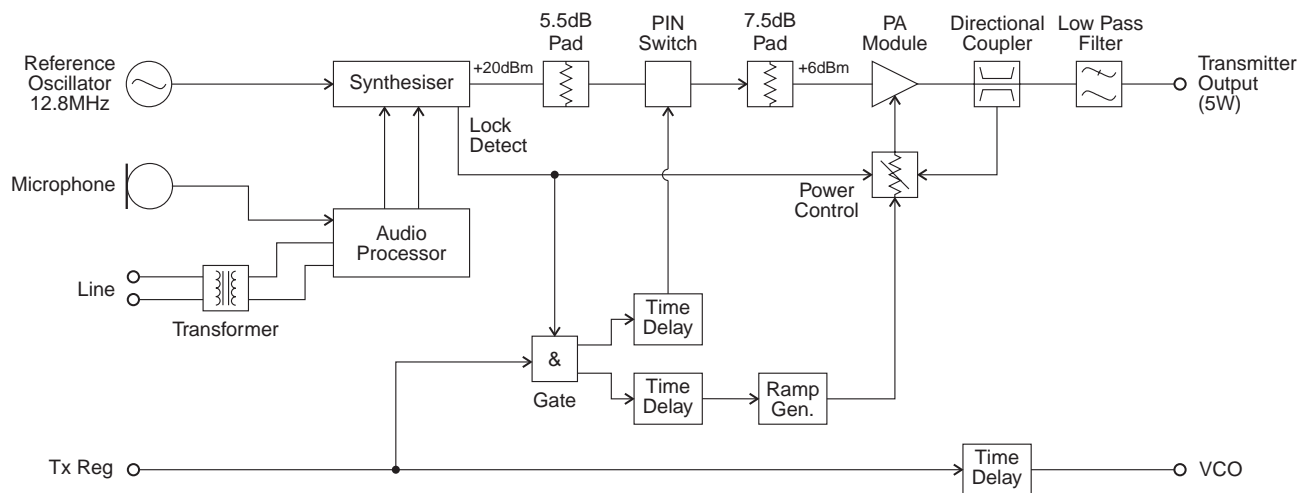

Figure 2.1   T881 High Level Block Diagram

2.2   Microcontroller

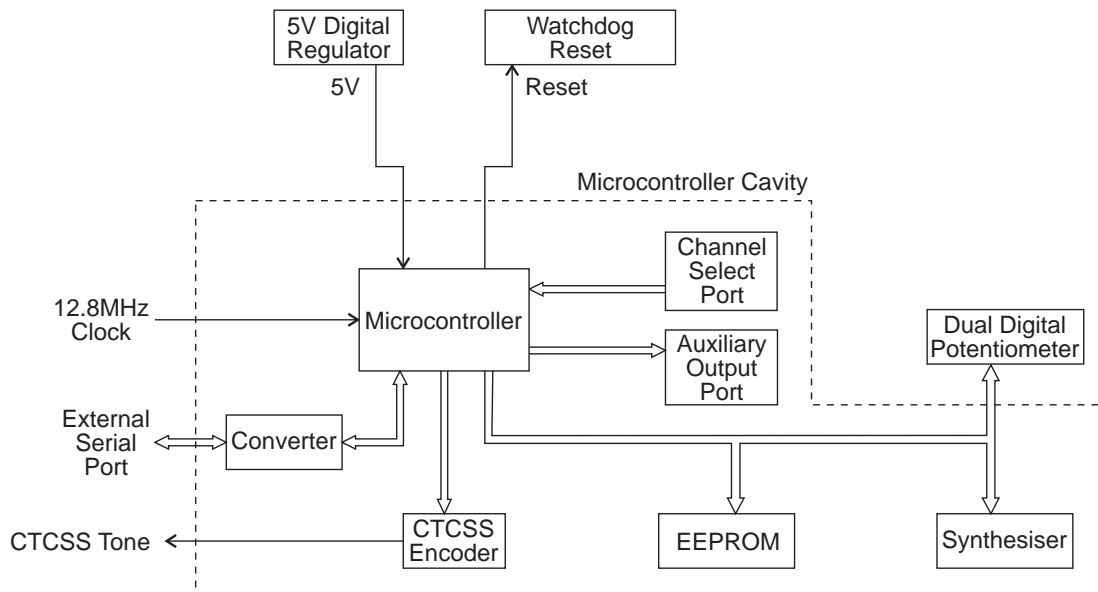(Refer to the microcontroller circuit diagram (sheet 8) in Section 6.2.)

Figure 2.2   T881 Microcontroller Block Diagram

Overall system control of the T881 is accomplished by the use of a member of the 80C51 family of microcontrollers (IC810). It runs from internal ROM and RAM, thus leaving all four ports free for input/output functions.

Non-volatile data storage is achieved by serial communication with a 16kBit EEPROM (IC820). This serial bus is also used by the microcontroller to program the synthesiser (IC740) and deviation control EPOTS (IC220).

The main tasks of the microcontroller are as follows:

- program the synthesiser and EPOT;
- interface with the PGM800Win programming software at 9600 baud via the serial communication lines on D-range 1 (PL100) & D-range 2;
- monitor channel change inputs from D-range 2;
- generate timing waveforms for CTCSS encoding;
- coordinate and implement timing control of the exciter/transmitter.
- control the front panel "Supply" LED.

2.3   Synthesised Local Oscillator

(Refer to the synthesiser circuit diagram (sheet 7) and the VCO circuit diagram (sheet 3) in Section 6.2.)
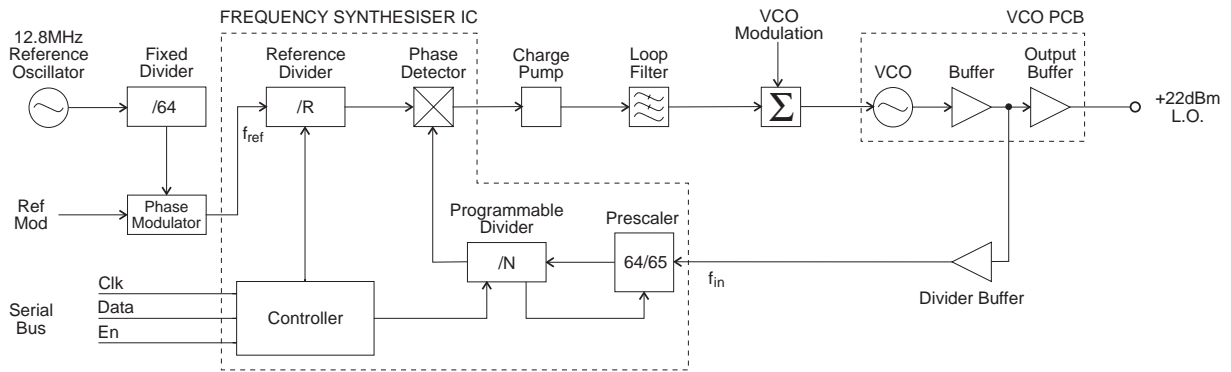

Figure 2.3   T881 Synthesiser Block Diagram

The synthesiser (IC740) employs a phase-locked loop (PLL) to lock a voltage controlled oscillator (VCO) to a given reference frequency. The synthesiser receives the divider information from the control microprocessor via a 3 wire serial bus (clock, data, enable). When the data has been latched in, the synthesiser processes the incoming signals from the VCO buffer (f_{in}) and the phase modulator (f_{ref}).

A reference oscillator at 12.8MHz (=IC700) is buffered (IC710 pins 5 & 6) and divided down to 200kHz (IC730). This 200kHz square wave is then summed with the modulating audio and passed to an integrator (IC720 pins 13 & 12, Q710, Q720). This produces a ramping waveform which is centred around a DC level determined by the incoming audio. IC720 pins 10 & 11 perform as a comparator, ultimately producing a phase-modulated 200kHz square wave. This is followed by another phase shifting stage (IC720 pins 8 & 9, Q730, Q740), before being divided down to 6.25kHz or 5kHz within the synthesiser IC (IC740).

A buffered output of the VCO (Q795) is divided with a prescaler and programmable divider which is incorporated into the synthesiser chip (IC740). This signal is compared with the phase modulated reference signal at the phase detector (also part of the synthesiser chip). The phase detector outputs drive a balanced charge pump circuit (Q760, Q770, Q775, Q780, Q785) and active loop filter (IC750 pins 5, 6 & 7, Q790) which produces a DC voltage between 0V and 20V to tune the VCO. This VCO control line is further filtered to attenuate noise and other spurious signals. Note that the VCO frequency increases with increasing control voltage.

If the synthesiser loop loses lock, a pulsed signal appears at LD (pin 2) of IC740. This signal is filtered and buffered by IC750 pins 1, 2 & 3, producing the Lock-Detect signal used to shut off the power supply to the drive amplifier. IC750 pin 1 is at 20V when the synthesiser is out of lock.

2.3.1   Two Point Modulation

Frequency modulation occurs by modulating both the VCO input and the synthesiser reference input. This process is called two point modulation and ensures a flat modulation response from 67Hz to 3kHz (2.55kHz for narrow bandwidth).

The PLL has a fast response time, allowing a Tx key-up time of <30ms. Because of this fast response time the PLL sees lower modulation frequencies superimposed on the VCO as an error and corrects for it, resulting in no modulation on the carrier. At modulation frequencies greater than 300Hz the loop cannot correct fast enough and modulation is seen on the carrier. The response of the loop to VCO modulation is shown by f_2 in Figure 2.4 below.

To achieve low frequency modulation, the reference oscillator is also modulated so that the phase detector of IC740 detects no frequency error under modulation. Thus, the synthesiser loop will not attempt to correct for modulation and the audio frequency response of the transmitter remains unaffected. The response of the loop to reference frequency modulation is shown by f_1 in Figure 2.4.

The reference modulation is controlled by a 256-step 10k electronic potentiometer (EPOT) which is adjustable via PGM800Win. The EPOT is made up of 256 resistive sections (representing approximately 39Ω each) which can be individually addressed by the microcontroller. Each section can be switched in or out of circuit to achieve the required total resistance, thus giving control of the reference modulation.
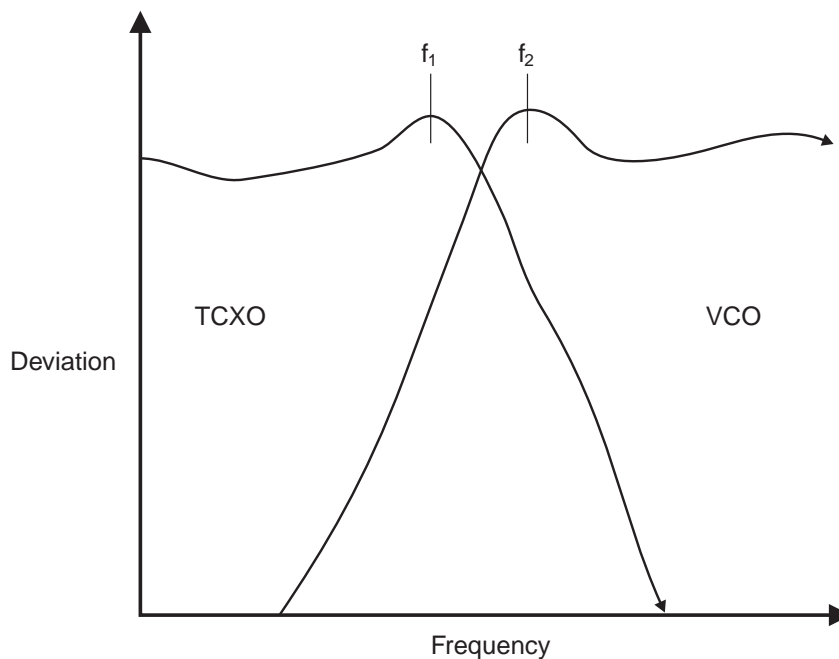

Figure 2.4   T881 Two Point Modulation

2.4   VCO

(Refer to the VCO circuit diagram (sheet 3) in Section 6.2.)

The VCO comprises the oscillator and three stages of buffer and gain to achieve the required power level and reverse isolation at the output of the VCO.

The oscillator transistor (Q309) operates in a common-base configuration, utilising a quarter-wave square ceramic resonator coupled between its collector and emitter to provide the feedback necessary for oscillation. The VCO control voltage from the loop filter (IC750) is applied to the varicaps (D300-D302) to facilitate tuning within an 8MHz band of frequencies. A high-Q sapphire trimcap (CV300) is used for coarse tuning of the VCO. The typical output power at the oscillator stage is 0dBm.

The output from the oscillator drives a cascode amplifier stage (Q302, Q303) which is designed to provide good reverse isolation from variable impedances of the following stages. The isolation of the circuit is typically 40dB, including 0-3dB of associated gain. An attenuated sample of the cascode output (Q302) is fed back to the synthesiser (IC640) through a divider buffer (Q795) for phase-locking.

Following the buffer is a broadband MMIC amplifier (Q308) which functions as a gain block to provide the drive to the final power stage (Q319). This stage typically provides approximately 10dB of gain.

The final stage of the VCO is a power amplification stage. The power transistor (Q319) and its associated circuitry increases the output power of the VCO to approximately +20dBm. The output power is then attenuated to +6dBm (approximately), which is the input level required to drive the RF power module.

Note: This power stage (Q319) is retained in the T881 transmitter to keep the VCO architecture the same as the T885 receiver, which does require a +20dBm output.

The VCO is an on-channel design, i.e. there are no multiplier stages to obtain the on-channel frequency. It is modulated by superimposing the audio signal onto the control voltage and by phase-modulating the reference signal.

2.4.1   VCO Supply

The VCO is supplied from two switched +9V supplies under the control of the Tx-Reg. supply.

The VCO and cascode amplifier are supplied from one +9V switched supply by Q321 via the C multiplier (Q316, C365).

The MMIC and final amplifier are supplied from the other +9V supply by Q314.

A delay circuit holds the VCO on for a short time after the Tx-Reg. supply has been switched off. This is to allow the RF power circuits to ramp down in the correct manner before the VCO is switched off.

2.5   Audio Processor

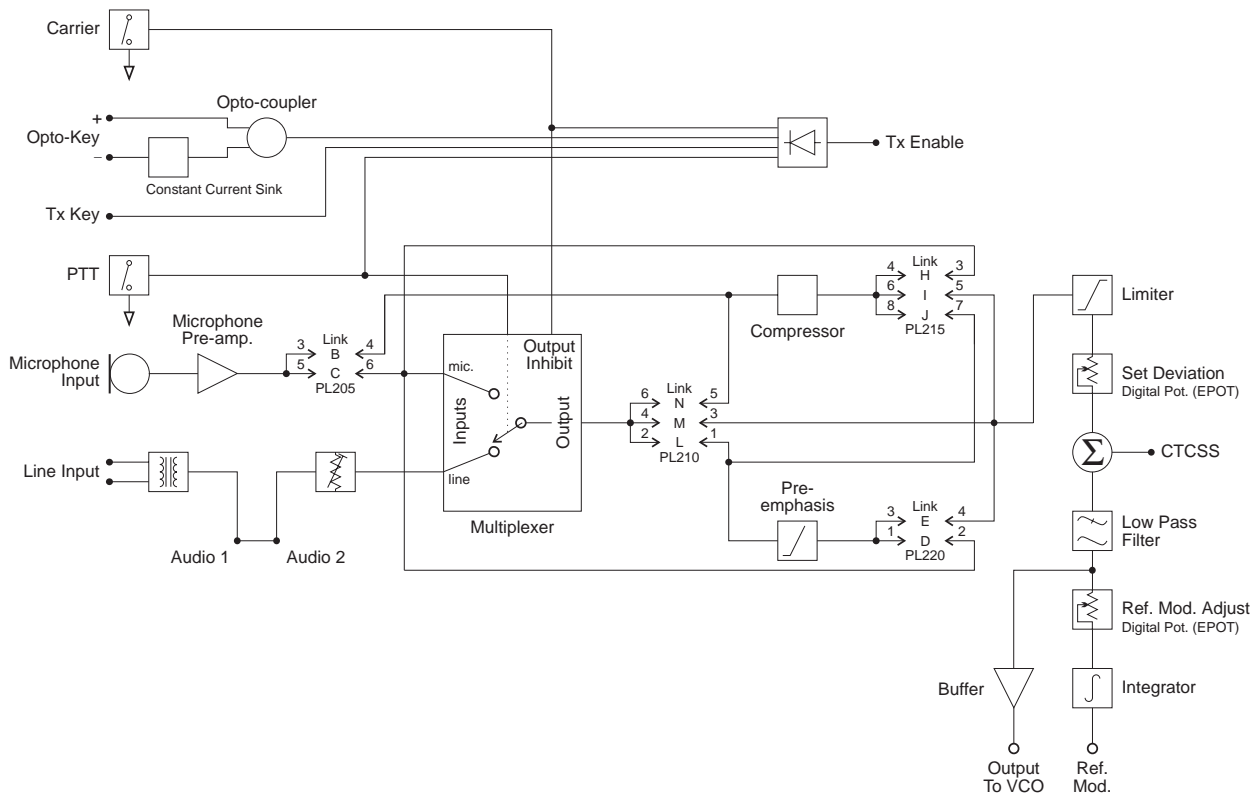(Refer to the audio processor circuit diagram (sheet 2) in Section 6.2.)

Figure 2.5   T881 Audio Processor Block Diagram

2.5.1   General

The audio processor comprises several link selectable circuit blocks which may be con-
figured in a variety of combinations to suit individual requirements. The pre-emphasis
network and compressor may be linked individually or cascaded between either or both
audio inputs and the limiter.

Refer to Section 3.5.1 for linking details.

2.5.2   Audio Inputs

Two audio inputs are available: one from a 600 ohm balanced (or unbalanced) line, and
the other from a local microphone. The microphone signal is passed first to a pre-ampli-
fier (Q210) and ultimately to a multiplexer (IC240), but in between may pass through
the compressor (depending on the linking details). The line transformer is also con-
nected to the multiplexer and is disabled by the microphone PTT switch.

A third input for external CTCSS tones is also provided.

2.5.3   Keying Inputs

There are four ways to key the exciter:

- pulling the Tx-Key line low (pin 13 on D-range 1 [PL100]) at the rear of the set);

- pushing the "Carrier" button on the front panel - this will inhibit all audio;

- using the PTT button on the local microphone, disabling audio from the line;

- via the opto-key inputs (pins 11 and 12 on D-range 1 [PL100]) when electrical isolation is required. This features a constant current sink (Q270) to ensure reliable activation of the opto-coupler (IC250) at low keying voltages.

2.5.4   Compressor (Automatic Level Control (ALC))

The input signal is fed via a current controlled attenuator (Q230, Q220) to a high gain stage (IC230) from which the output signal is taken. This signal is passed to a comparator (IC230) which toggles whenever the audio signal exceeds a DC threshold determined by RV220. Thus, the comparator produces a square wave whose mark-space ratio is determined by the amplitude of the audio signal. This square wave pumps up the reservoir capacitor (C233) which controls the attenuator (Q230, Q220), thus completing the feedback loop.

The compression level is set by adjustment of the comparator threshold (RV220).

Note: Although the high dynamic range of the compressor allows the use of very low audio signal levels, such conditions will be accompanied by a degradation of the signal-to-noise ratio. Very low audio input levels should therefore be avoided where possible.

2.5.5   Outputs To Modulators

The output signal from the limiter (IC210, IC230) is summed with a CTCSS tone at a summing amplifier (IC260). The signal is then low pass filtered (IC260) and split to supply the two modulators.

Since the VCO modulator is a true frequency modulator, its audio is simply buffered (IC260). The reference modulator, however, is a phase modulator and its audio must first be integrated (IC210).

It is vital that the audio levels to the modulators are accurately set, ***relative to each other***. Hence the inclusion of level adjustment in the reference modulator path. Once set, adjustments to absolute deviation may be made only by IC220, a 256-step 10k electronic potentiometer (EPOT), which is controlled via PGM800Win. The EPOT is made up of 256 resistive sections (representing approximately 39Ω each) which can be individually addressed by the microcontroller. Each section can be switched in or out of circuit to achieve the required total resistance, thus adjusting the absolute deviation level.

2.6   Power Supply & Regulator Circuits

(Refer to the regulators circuit diagram (sheet 6) in Section 6.2.)
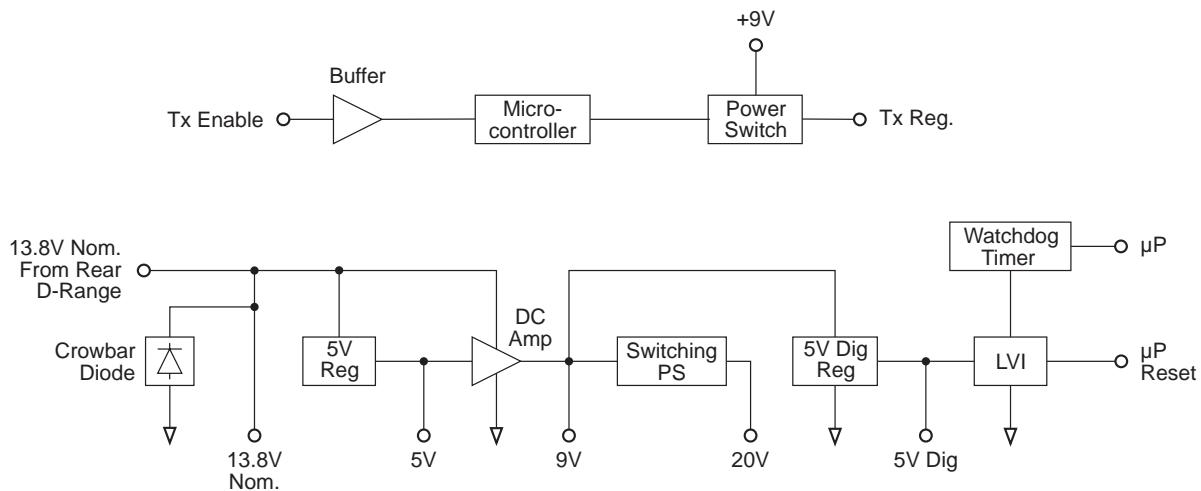

Figure 2.6   T881 Power Supply & Regulators Block Diagram

The T881 is designed to operate from a 10.8-16V DC supply (13.8V nominal). A 5.3V regulator (IC630) runs directly from the 13.8V rail, driving much of the synthesiser circuitry. It is also used as the reference for a DC amplifier (IC640, Q630, Q620) which provides a medium current capability 9V supply. The T881 has a regulator (IC370) which produces 9V for use in the exciter and audio circuits.

A switching power supply (Q660, Q670) runs from the 9V supply and provides a low current capability +20V supply. This is used to drive the synthesiser loop filter (IC750), giving a VCO control voltage range of up to 20V.

Ultimate control of the transmitter is via the Tx-Reg. supply, switched from 9V by Q610. This is enabled via the Tx-Enable signal from the audio processor, and microprocessor.

A crowbar diode is fitted for protection against connection to a power supply of incorrect polarity. It also provides transient overvoltage protection.

Note: A fuse must be fitted in the power supply line for the diode to provide effective protection.

2.7   Transmit Timers

The transmit tail timer, transmit timeout timer and transmit lockout timer can all be set from PGM800Win. The fields for setting these are found on the system information page. These three timers operate as follows (refer also to Figure 2.7):

| Timer	Function	Adjustment
Transmit Tail	Sets the tail time during which the transmitter stays keyed after the external key source has been removed.	0-5 seconds in 20ms steps
Transmit Timeout	Sets the maximum continuous transmission time. Once the timer has timed out, the transmitter must be keyed again, unless prevented by the transmit lockout timer.	0-600 seconds in 10 second steps
Transmit Lockout	Sets the period of time that must elapse after a timeout before the transmitter can re-transmit. Once the timer has timed out, the transmitter can be keyed again.	0-60 seconds in 10 second steps
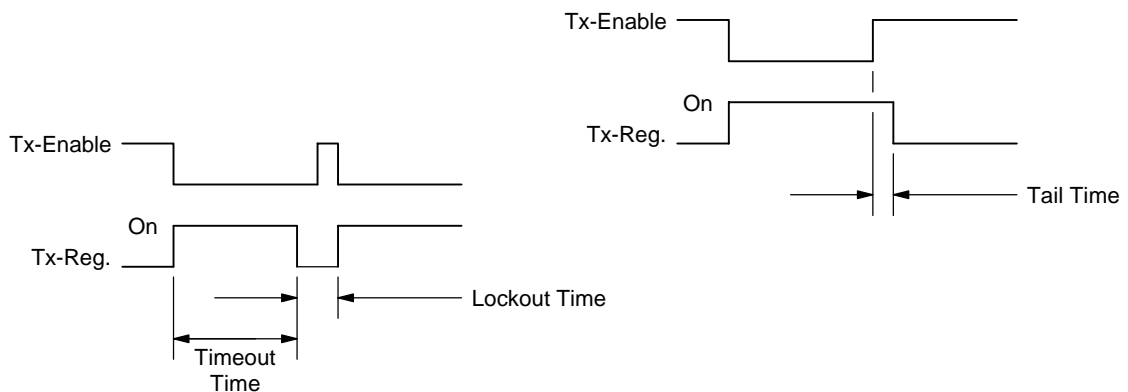
Figure 2.7   T881 Transmit Timers

2.8   Power Control Circuit & PA

(Refer to Figure 2.1 and the power control and PA circuit diagrams (sheets 5 & 4) in Section 6.2.)

The output power of the PA is maintained at a constant level via a power control loop applied to the bias pin of the RF power module (#IC400 pin 2). The forward and reverse RF power levels are sensed via a dual directional coupler and detector diodes (D400, D402 in the PA cavity). The detected DC signals are buffered (IC500 pins 3 & 5), summed with a very small bias current and then fed to the control integrator op-amp (IC510 pin 9). The purpose of the small bias current (provided by R559) is to raise the voltage potential slightly at the summed node. This is necessary to ensure the output voltage at IC510 pin 8 is zero when the transmitter is not keyed on.

Note: Forward and reflected power signals are summed so that, under high VSWR, the power control will turn the output RF level down.

To reduce the spurious output level when the synthesiser is out-of-lock, the Tx-Reg. and Lock-Detect signals are gated to inhibit the PA control circuit and to switch off the RF signal at the input to the RF power module. This is achieved by a PIN diode switch (D308). There is a 5.5dB (R370, R372, R383) and a 7.5dB (R390, R391, R392) pi-attenuator at the input and output of the PIN switch to attenuate the level of the VCO output and also provide good isolation between the VCO and RF power module. A level shifter is also implemented to enhance the transient performance by improving the dynamic range of the module bias voltage.

Cyclic keying control is provided by additional circuitry consisting of a ramp, several gate and time delay stages:

- Q505, Q508, IC510   trapezoidal power ramping generator
- Q500, Q501   Tx-Reg. and $\overline{\text{Lock-Detect}}$ gate
- Q502, Q506, Q510, Q512, Q513   PIN switch drive plus delay
- Q507, Q511, Q515   level shifter plus delay.

This is to allow the RF power circuits to ramp up and down in a controlled manner so that minimal adjacent channel interference is generated during the transition.

A temperature sensor (R450) is mounted on the input flange of the RF power module to monitor the flange operating temperature. When a pre-determined temperature threshold is exceeded, a protection circuit (IC510 pin 7, Q516) switches on to reduce the RF output power to a preset level. The purpose of the protection circuit is to prevent overheating, as the RF power module is rated for a maximum flange temperature of 100°C.

The RF power module is a 5W device which requires an input drive of approximately +6dBm. L402 and C430 are provided to match the impedance of the output low pass filter to the impedance of the module. A DC control signal is applied to the RF signal path via %L405 if cyclic keying is required with a Tait power amplifier.